Modeling and Experimental Demonstration of Accelerated Self-Healing Techniques

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Aging/Wearout

- Process, Voltage, Temperature and Aging (PVTA) variations
- Parametric (e.g. $V_{th}$, $\mu$, $g_m$) shift over time
- Both Irreversible (e.g. HCl) and Reversible (e.g. BTI)

Reversible (e.g. BTI)

![Diagram of circuit and timing error with high power and failure]

$\Delta V_{th}(t_1) = V_{stress} - V_{stress - Remove}$

$\Delta V_{th}(t_2) = V_{stress} - V_{stress - Remove}$
Previous Work

• Accept the variations, track and monitor them, then adapt to them (Design for worst case)
  T. Kim et al. [JSSC ’08], A. Cabe et al. [ISQED ’09],
  Z. Qi et al. [GLVLSI ’09], S. Kumar et al. [ASP-DAC ’09]

• Reduce/Repair aging-induced variations
  Stress Phase: L. Zhang et al. [ASP-DAC ’09], J. Shin, et al. [ISCA ’08]
    S. Gupta, et al. [ASP-DAC ’12][TODAES ’13]
  Recovery Phase: Active Recovery (This work)

Accelerated Self-Healing
Accelerated Self-Healing

• Inspired by Biology: Sleep vs. Inactivity
  Old: Sleep = Inactivity
  New: Sleep = Active Recovery

• Sleep Conditions
  Temperature, Supply Voltages

• Proactive Recovery
  Active/Sleep Ratio

Hypothesis: Rejuvenate the chip by explicitly controlling the *Ratio of Active vs. Sleep* and *Sleep Conditions* (e.g. *Higher temperatures, Negative voltage Supply*)

*Source: http://gladstoneinstitutes.org/node/11312*
Cross-Layer Model

- Based on Trapping/Detraping (J. Velamala et al. [DAC ’12])
- Both stress phase and accelerated recovery phase
- Use delay change as the metric
- Fitting parameters are extracted based on measurement

\( t_1 \): Stress time; \( t_2 \): Recovery time

The total threshold voltage shift:
\[
\Delta V_{th}(t_1 + t_2) = \phi_2 (A + \log(1 + Ct_2)) + \Delta V_{th}(t_1)(1 - \frac{k + \log(1 + Ct_2)}{k + \log(1 + C(t_2 + t_1)})
\]

\( \phi_2 \sim K_2 \exp(-E_0^\circ \exp(\frac{BV_{dd}}{kT})) \)

The delay of a digital gate:
\[
t_d \sim \frac{C_L V_{dd}}{I_d} \ll \frac{C_L V_{dd}}{V_{dd} - V_{th}} \quad \rightarrow \quad \Delta t_d \sim \frac{\Delta V_{th}}{V_{dd} - V_{th}} \cdot t_{d0}
\]

The total delay change:
\[
\Delta T_d (t_1 + t_2) = \phi_2 t_{d0} \frac{(A + \log(1 + Ct_2))}{V_{dds}} + \Delta T_d (t_1)(1 - \frac{k + \log(1 + Ct_2)}{k + \log(1 + C(t_2 + t_1)})
\]

Delay change in one cycle (t):
\[
\Delta T_d (t) = \phi_d t_{d0} \frac{(A + \log(1 + C \frac{t}{1 + \alpha}))}{V_{dds}} + \Delta T_d (\frac{\alpha t}{1 + \alpha})(1 - \frac{k + \log(1 + C \frac{t}{1 + \alpha})}{k + \log(1 + C \frac{t}{1 + \alpha})}
\]
Experimental Validation on FPGAs (40nm)

- Accelerated testing methodology
- Ring oscillator based test structure
- Knobs: voltage, temperature, switching activity (AC/DC) and Ratio of active and sleep time.
- 11 Test Cases

Test configuration

\[ T_d = \frac{1}{2 \cdot f_{osc}} = \frac{1}{4 \cdot C_{out} \cdot f_{ref}} \]
Stress Phase Results

- Effect of Switching Activity on aging (T=110°C, 50% Duty Cycle)

- Recovery is at a much slower rate → AC stress degrades the performance at a slower rate

- Effect of temperature on performance degradation (%) for DC stress

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Measurement</th>
<th>Model</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>12 hours</td>
<td>24 hours</td>
</tr>
<tr>
<td>20</td>
<td>0.13%</td>
<td>0.19%</td>
</tr>
<tr>
<td>100</td>
<td>1.1%</td>
<td>1.5%</td>
</tr>
<tr>
<td>110</td>
<td>1.45%</td>
<td>2.16%</td>
</tr>
</tbody>
</table>
Recovery Phase Results

- **Negative Voltage** ($V_{dd} = -0.3V$)

- **High Temperature** ($T = 110^\circ C$)

\[ = \text{Delay(0)} - \text{Delay(t)} \]

**Graphs:**
- Recovered Delay vs. Time for different conditions.
- Comparison of model predictions vs. experimental results.

**Legend:**
- $0V$ vs. $-0.3V$
- $20^\circ C$ vs. $110^\circ C$
- Model vs. Experimental Data
Model vs. Measurement

- Recovery Phase
- Model predicts the same trend
Proactive Recovery

• Ratio of active to sleep time = 4

• Summary (Recovered Percentage %)

<table>
<thead>
<tr>
<th>Case</th>
<th>Measurement(%)</th>
<th>Model(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20°C and 0V</td>
<td>0.66%</td>
<td>1%</td>
</tr>
<tr>
<td>20°C and -0.3V</td>
<td>16.7%</td>
<td>14.4%</td>
</tr>
<tr>
<td>110°C and 0V</td>
<td>28.7%</td>
<td>29.6%</td>
</tr>
<tr>
<td>110°C and -0.3V</td>
<td><strong>72.4%</strong></td>
<td>70%</td>
</tr>
</tbody>
</table>

T=110 °C, Vdd=-0.3V

Active/Sleep=4
Potential Applications

• On-chip solution
  - Negative Voltage
  - On-chip Heater (Utilize Dark Silicon)

• Exploring other sources to accelerate recovery

• Reverse other aging mechanisms (e.g. EM)
Conclusion

- Three accelerated self-healing techniques (Inspired by biology)
  - Sleep conditions
    - High Temperature, Negative Voltages
  - Proactive recovery (Schedule active vs. sleep)
- Modeling and experimental demonstration
- Potential applications (e.g. Multicore)

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