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Overview

Wearout Issues

- BTI, HCI, TDB, EM, etc.
- Increase design margin and worsen metrics
- Cross-layer issues
- Both Reversible and Irreversible Part

Previous Solutions

- Tolerate - Design for the worst case
- Compensate - Dynamically adapt to wearout
- Slow - Reduce the stress during operation
- Passive Recovery

This Work

- Repair wearout completely
- Accelerated & Active Recovery
- Circadian Rhythms for FULL recovery
- Introduce Accelerated & Active Recovery as a new design knob for cross-layer resilience

Accumulated Self-Healing [DAC '14]

Main Ideas

- Sleep → Proactive Recovery
- Some of the effects of wearout (e.g. BTI and EM) can be reversed by applying several techniques (high temperature, negative voltage, UV light, reverse current, etc.), thus leading to an effective accelerated self-healing fundamentally.

Test Setup

- Commercial 40nm FPGA chips
- Accelerated Testing Methodology
- Knobs: V, T, AC/DC, Sleep/Active

Results

- Commercial 40nm FPGA chips
- Accelerated Testing Methodology
- Knobs: V, T, AC/DC, Sleep/Active

“Sleep When Getting Tired” [ASPDAC ’16]

Main Ideas

- The boundary between reversible & irreversible is “soft”
- Irreversible wearout can be recovered through acceleration
- Frequency dependency of accelerated wearout & recovery
- “Sleep when getting tired” to FULLY avoid the irreversible wearout
- Negative “turbo” boost at the system level

Results

- An identical regular operation case (31 hours vs. 16 hours)
- To the 1st vs. 16 accelerated stress case for FULL recovery

Architecture-level Implementations

Main Ideas

- Utilize the intrinsic heat
- Active blocks heal inactive elements
- Utilize core redundancy and/or Dark Silicon
- Shift the workload among cores

System-level Implementations

Scheduling/Load-balancing

- System scheduler schedules the recovery proactively based on the known circadian rhythms (e.g. for mobile device applications, 12 hrs + Sleep time)

Wearout-FREE System

- Full Recovery time (under different sleep conditions) after 12-hour constant stress under regular operation condition (no accelerated stress)

Tech Transfer

Industry Interactions

- Acknowledge industry liaisons: Tanay Karnik (Intel), Matthew Ziegler (IBM)
- Send updates regularly
- Discuss at SRC annual reviews

Publications/Presentations

- DAC ’14, SELSE ’15, ASPDAC ’16
- VLSI, the Integration Journal
- DAC ’15, ASPDAC ’16 PhD Forums, GOMAC Tech ’15
- Two more papers to be submitted