

Dependence of Recognition Accuracy on Available Network Bandwidth

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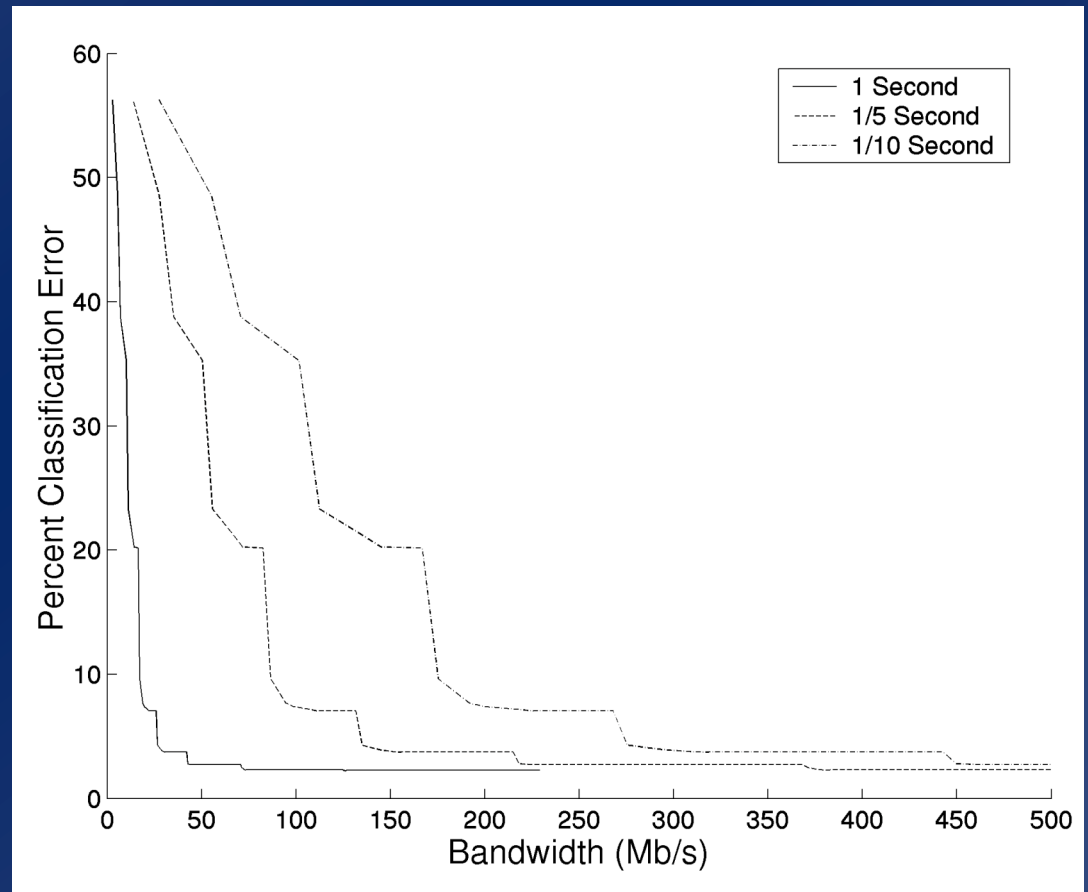


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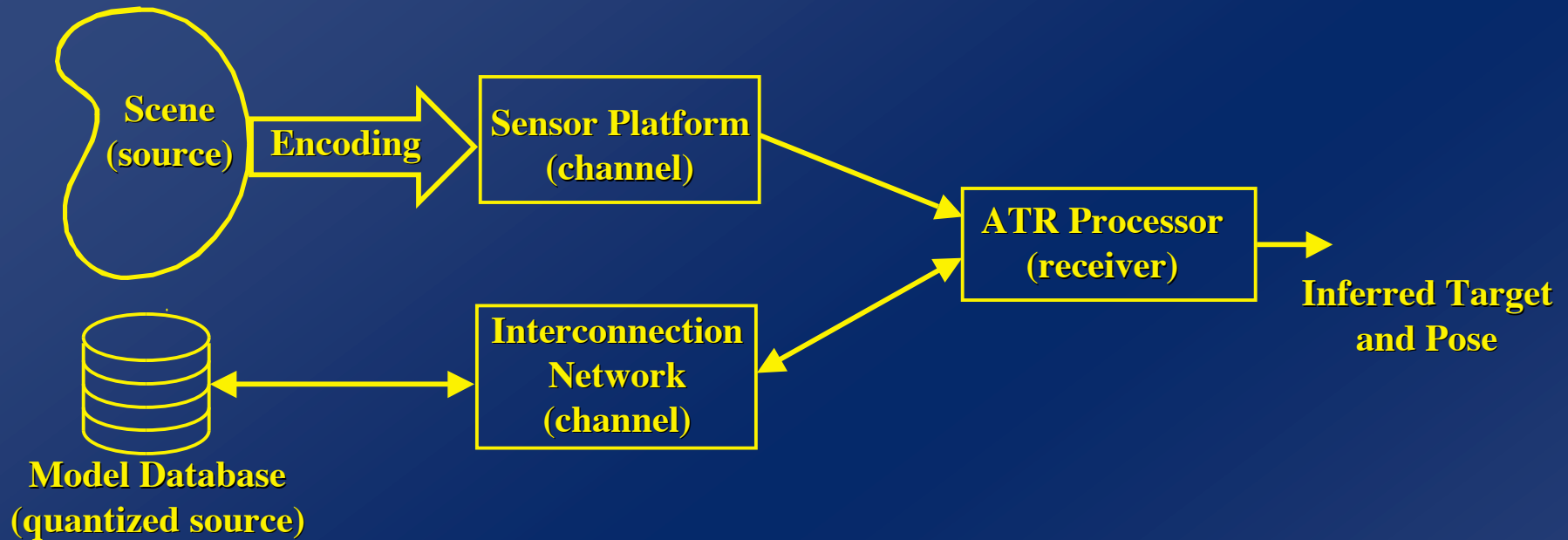
Summary

- **Recognition Accuracy is Resource Dependent**
- **Varying Resource Availability**
 - Resource Reallocation
 - Changing Environment or Requirements
 - System Damage
- **Dynamic Application Reconfiguration**
- **Successively Refinable Data Representations**
- **Application to SAR ATR**



Classification Errors vs. Available Bandwidth

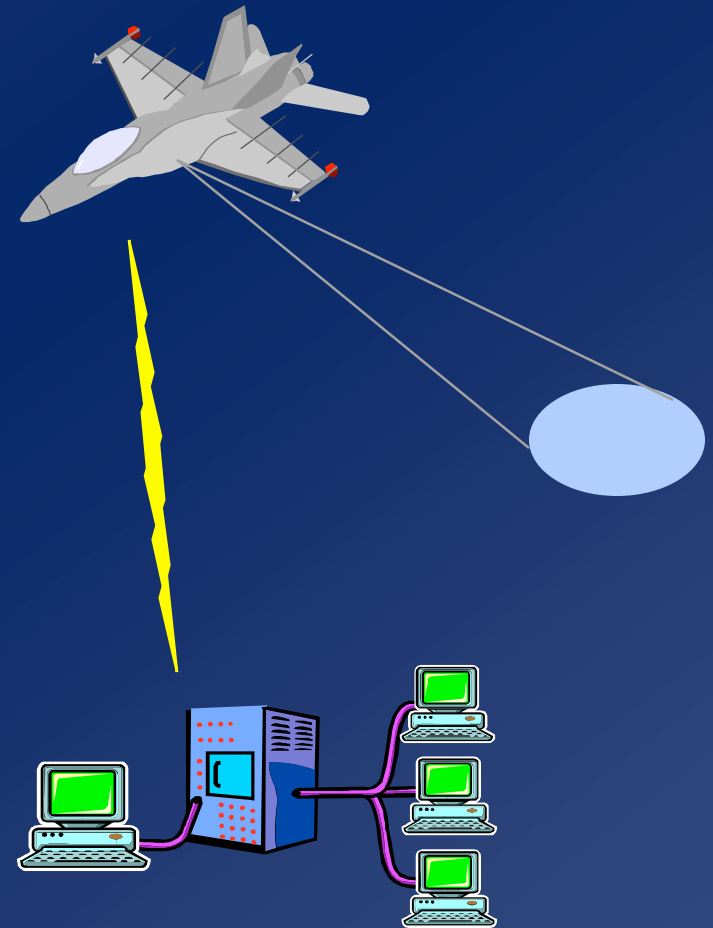
Accuracy and Resource Consumption



- **ATR processing consumes network and computation resources**
- **Accuracy depends in part on data representation complexity**
 - Truer representation allows closer to optimal results
- **Resource consumption depends in part on data complexity**
 - Higher complexity can mean more data to process
- **Dynamic adjustment of data representation complexity to accommodate variation of available resources**

Data Communication Rates

- **Rate of data a measure of information to the processors per classification**
- **Required average classification time sets rate in bits per second**
- **Sensor data gathered for analysis**
 - Processors may be remote
 - Sensor data may be stored for later analysis
- **Model data retrieved during recognition**
 - Data storage bus may be shared
 - Database and/or processors may be distributed

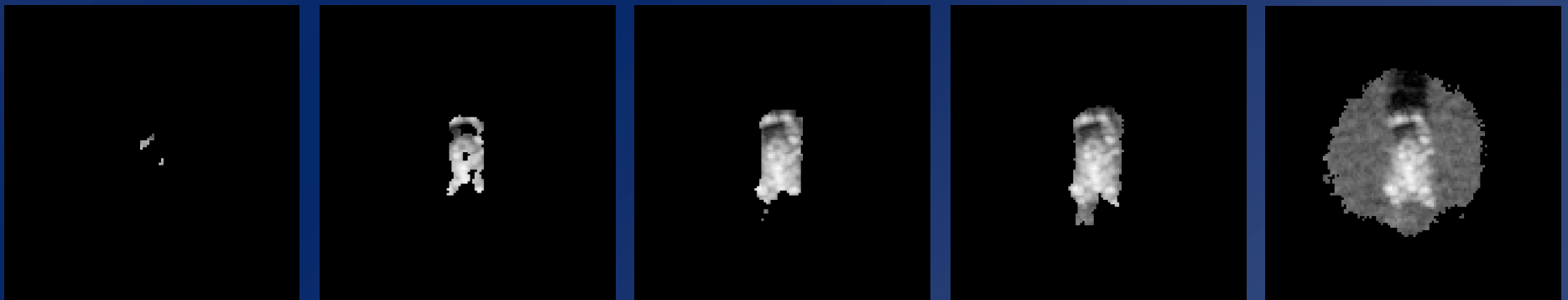


Other Resource Consumption Rates

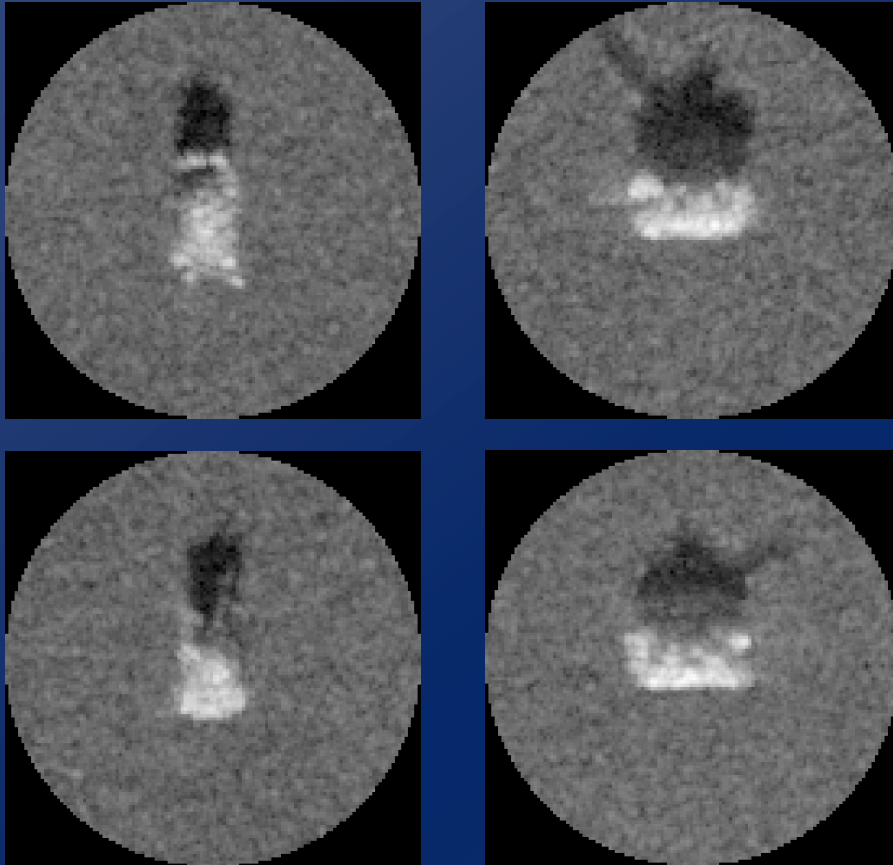
- **Network bandwidth is one of many types of resources**
- **Other average rates of resource consumption:**
 - Elapsed time per classification
 - CPU cycles per classification
 - Database (magnetic) storage per model class
 - Power dissipation
- **ATR processor may be one module in a larger system**
 - Process on a shared computing platform
 - Network of embedded recognition systems
- **Changing resource consumption rates due to:**
 - Variation in application requirements
 - Reallocation of resources to higher priority tasks
 - Damaged or offline computation elements
 - Disrupted communication paths
 - Power considerations

Successively Refinable Data Representations

- **Dynamic reconfiguration through successively refinable data representations**
- **Process incrementally more complex representations until:**
 - a classification is required
 - resource allocation exhausted
- **Example of successively selecting SAR pixels based on information content relative to clutter, $D(p_{\text{pixel}} \parallel p_{\text{clutter}}) > \gamma$**



Signature Variation



Model data varies with:

- **Pixel location**
- **Target class**
- **Pose**
- **Orientation relative to sensor platform**

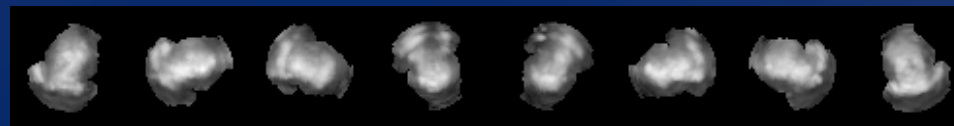
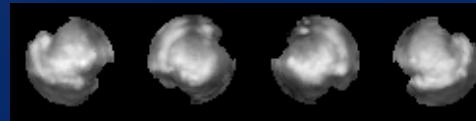
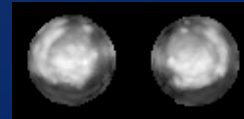
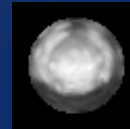
Variance in SAR pixels with orientation

Hierarchical Model Families

Successive refinement in orientation

Statistics over decreasing intervals of widths $2\pi, \pi, \dots, 2\pi/2^{m-1}$

Approximate variance
images for bulldozer (D7)
from 2π through $\pi/8$



Successively-refinable
models yield successively-
refinable decisions

Resource consumption depends on extent of search (complexity)

Hardware Modeling

- **ATR by maximizing the likelihood function**

$$L(\theta) = \prod_{i=1}^N \frac{1}{\sigma_i} \exp\left(-\frac{|x_i - \mu_i|}{\sigma_i}\right)$$

- **Time to classify image of an unknown object includes:**
 - Time for image distribution to all available processors

$$T_{\text{dist}} = \frac{N \cdot L}{P}$$

- Time to retrieve model data for each approximation

$$T_{\text{model}} = \frac{N \cdot M}{P}$$

- Time to evaluate log-likelihood

$$T_{\text{eval}} = \frac{N \cdot (L + M)}{P}$$

Network Dependence

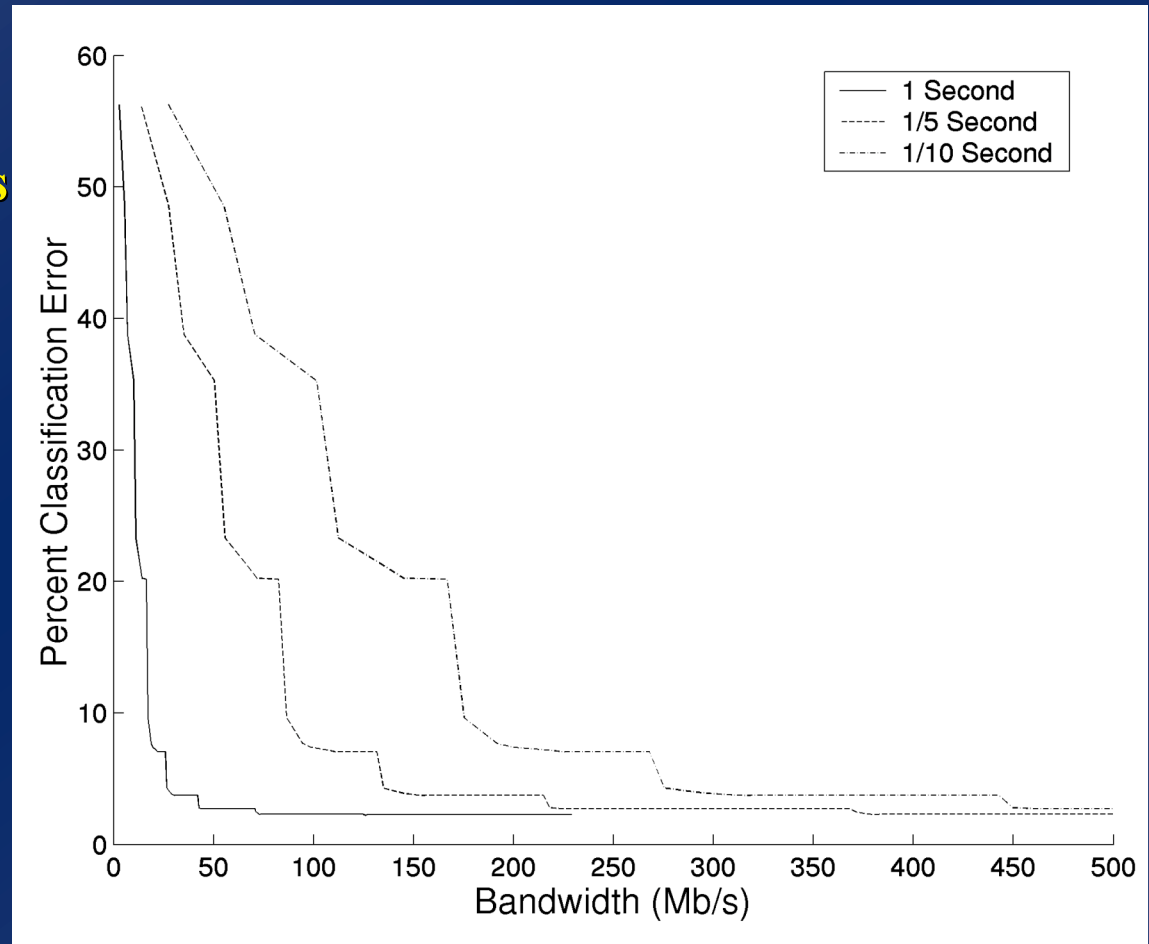
- Experimentation yields empirical error as a function of model complexity
- Sample data yields empirical number of bits as a function of model complexity
- Hardware model yields classification time as a function of model complexity
- For fixed classification time, bandwidth required to support complexity c is

$$BW(c) = \frac{c}{T}$$

- Plot Error(c) vs. BW(c) for fixed classification time

Analysis Results

- **Ten-class results on actual SAR data**
- **Assumptions**
 - 4 superscalar processors
 - 1 GHz clock
 - 0.5 CPI
- **Research – compare competing algorithms**
- **Design – bandwidth required for ATR**
- **Operation – Decline in bandwidth requires larger error or slower classification**



Conclusions

- **Dynamic application reconfiguration accommodates changing availability of hardware resources**
- **Hierarchical data representations allow optimization over increasingly complex spaces**
- **Model for hardware united with empirical performance data**
- **Results useful in research, development, and operational phases**

Research Goals

- **Development of rate-recognition theory**
 - **Rate of sensor data**
 - **Rate of model data**
- **Representations that capitalize on limited hardware resources**
 - **Network throughput**
 - **Computational capability**
 - **Power consumption**