We are deep in a multi-dimensional calculation where it is very easy to lose track of details and direction.

So let's back off for a moment and take stock:

We have built a metal / oxide / semiconductor CAPACITOR

Want to apply voltage to top plate, inducing counter-charge in semiconductor bottom plate

If it were a simple capacitor, we'd have this situation:

\[
\begin{array}{c|c|c}
\text{Metal} & \text{Oxide} & \text{Metal} \\
\hline
+ & - & - \\
+ & - & - \\
\end{array}
\]

With a corresponding plot of voltage (potential energy per positive charge) vs. position:

\[
\text{Indicating positive charges would move right}
\]

\[
\text{Voltage (x)} \quad x
\]

However, in our MOS capacitor, the right plate is not thin, it is the semiconductor's "depletion layer."

Depletion layer's charge is the acceptor - (donor+) ions left behind after it was depleted of holes (electrons)

Charge, according to "Poisson's Equation" implies CURVATURE OF VOLTAGE:

\[
\nabla \xi = \frac{\rho}{\varepsilon} \\
\n= \nabla^2 V = \frac{\rho}{\varepsilon}
\]

Which means our MOS capacitor must be modified as follows:

\[
\begin{array}{c|c|c|c}
\text{Metal} & \text{Oxide} & \text{Semiconductor} \\
\hline
+ & - & - \\
+ & - & - \\
\end{array}
\]

Giving corrected voltage and electron energy plots that would look like this:

\[
\text{Curvature begins as enter depletion layer charge}
\]

\[
\text{But within gap, as move from oxide INTO semiconductor, there is an additional abrupt change in energy:
}

\[
\text{Due to differences in oxide and semiconductor electron affinities} \Rightarrow \text{Charge dipole layer at boundary}
\]

\[
\text{Finally giving us:}
\]

\[
\text{Which corresponds directly to the upper lines in our electron energy plot from last hour:}
\]

And electron energy vs. position:

\[
\text{But electrons would go left!}
\]

But within gap, as move from oxide INTO semiconductor, there is an additional abrupt change in energy:

\[
\text{Due to differences in oxide and semiconductor electron affinities} \Rightarrow \text{Charge dipole layer at boundary}
\]

\[
\text{Finally giving us:}
\]

\[
\text{Which corresponds directly to the upper lines in our electron energy plot from last hour:}
\]
Step #0: Isolated materials

Step #1: Assemble stack (look quickly before reaches equilibrium!)

EF_metal > EF_semi  \( \xi = 0 \) Everywhere!
EF_metal < EF_semi

Step #2: Allow to come to equilibrium (\( V_{app} = 0 \))

Step #3: Apply external voltage to metal gate = \( V_{FB} \) ("V flat-band")

Step #4: Apply additional voltage to INVERT the semiconductor surface

Hold it! Are we going in circles: Step #1 (assemble) = Step #3 (flat band)

Not really: Step #1 (assemble) = Imaginary (cannot look that quickly)
Step #3 (flat band) = Experimentally possible = Reference point

Step #4 = THRESHOLD of surface inversion
Defined as condition when charge density at semiconductor surface = charge density (of opposite type!) deep in semiconductor

REQUIRES:
\[ |E_F - E_i|_{surface} = |E_F - E_i|_{deep in semiconductor} \]

V_{applied} = \( V_{metal} - V_{semi substrate} \) Producing this condition = \( V_{Threshold} \)

\[ V_T = \text{Voltage to flatten bands (} V_{FB} \text{)} \]
\[ + \text{Additional voltage to invert semi. surface (} 2 \phi_{Fp} \text{ or} -2 \phi_{Fn} \text{)} \]
\[ + \text{Voltage drop in oxide} \]
OK, but what is $V_{ox}$ (part of applied voltage dropped across oxide)?

Oxide = Core of a capacitor (with metal / semiconductor = plates)

For which $Q = CV$ holds:

- Capacitance: $C_{ox} = \frac{c_{ox} A}{T_{ox}}$
- Capacitance / Area: $C'_{ox} = \frac{H_{ox}}{T_{ox}}$

For this capacitor:

$$V = V_{left} - V_{right} = Q_{left} / C - Q_{right} / C$$

$$= -Q_{depletion\ layer\ in\ semiconductor} / C'$$

$$= q N_a x_{dt} / C' \text{ P-semi} \quad \text{or} \quad -q N_d x_{dt} / C' \text{ N-semi}$$

Charge =

- total depletion layer
- charge in semiconductor

Giving a complete expression for $V_T$ (assuming an ideal oxide - for real oxide correction, see page 12 below):

N-Channel MOSFET: Ideal oxide & P-semi

$$V_T = V_{metal} - V_{semi}$$

$$= V_{FB} + 2 I_{fp} + V_{ox} \quad (P-semi \Rightarrow N-channel)$$

P-Channel MOSFET: Ideal oxide & N-semi

$$V_T = V_{metal} - V_{semi}$$

$$= V_{FB} - 2 I_{fn} + V_{ox} \quad (N-semi \Rightarrow P-channel)$$

Where $Q_{sd(max)}$ = semiconductor depletion charge / area

"max" because for $V$ beyond inversion, additional voltage >> more drop across inversion layer

$$= \sim \text{very little further growth of depletion layer beyond width } x_{dt}$$

Use:

$$C'_{ox} = \frac{c_{ox}}{T_{ox}} = \frac{k_{ox}}{T_{ox}}$$

With $\phi$'s defined as positive:

$$I_{fp} = \frac{(1/q) (E_i - E_F)}{kT/q}$$

$$I_{fn} = \frac{(1/q) (E_F - E_i)}{kT/q} = (kT/q) \ln (N_a / n_i) = (kT/q) \ln (N_d / n_i)$$

And recalling that for ideal oxide $V_{FB}$ (which corrects for $E_F$ mismatch):

$$V_{FB} = \phi_{ms} = \phi'_{m} - \phi'_{semi}$$

Best real oxide = $SiO_2$ grown by heating Si in oxygen (Frosche's accident)

Despite disorder inside $SiO_2$, there IS bonding => ~ No charge in bulk of oxide

I keep on inserting ideal oxide, smell a rat? Ideal oxide = One containing no charge

Real oxide = Amorphous (disordered / non-crystalline)
However:

1) At boundary between disordered SiO$_2$ and crystal Si get dangling bonds => charge
2) Positive ions (e.g. Na$^+$) can move through SiO$_2$ and get trapped near SiO$_2$/Si interface

Result: Sheet of positive charge at or near SiO$_2$/Si interface

Old all encompassing notation = $Q'$ss = $Q'$surface states
Newer notation = breaks up $Q$ into types (interface ...)

Metal

Oxide

Semiconductor

\[ \text{MOS capacitor} \]

Typical value of $Q'_{ss}$

\[ \text{is} \ - 10^{10} \text{q/cm}^2 \]

\[ \text{NEW! negative charge induced on metal gate = changes } V_T: \]

\[ \text{minus} \ < \ \text{field} \ + \ \text{plus} \]

\[ \text{But } \xi \nabla V \]

\[ \text{thus inside oxide voltage is increasing toward semi:} \]

From oxide as capacitor

\[ \Delta V_{oxide, ss} = \frac{Q'_{ss}}{C'_{ox}} \]

Re-evaluating flat band condition

\[ V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C'_{ox}} \]

Or:

\[ V_{FB} = \phi_{ms} - \frac{Q_{ss} \cdot T_{ox} \cdot Q'_{ss}}{\varepsilon_{ox}} \]

Significance, term by term, (for N-MOSFET expression):

\[ V_T = - \left( \frac{Q'sd(max) + Q_{ss}}{C'_{ox}} \right) + \phi_{ms} + 2 \phi_{fp} \]

Correcting our earlier $V_T$ summary (for MOSFETs with REAL oxides containing interface charge):

\[ \text{N - Channel Enhancement Mode MOSFET} \]

\[ \text{(metal / oxide / N-inversion layer on P-Semi)} \]

\[ V_T = V_{metal} - V_{semi} \]

\[ = V_{FB} + 2 \phi_{fp} + V_{ox \_p \_depletion} \]

\[ = V_{FB} + 2 \phi_{fp} + q N_a x_{depletion} / C'_{ox} \]

\[ = V_{FB} + 2 \phi_{fp} \cdot Q'_{sd}(max) / C'_{ox} \]

\[ = - \left( Q'sd(max) + Q_{ss} \right) / C'_{ox} \cdot \phi_{ms} + 2 \phi_{fp} \]

Where:

\[ C'_{ox} = \frac{c_{ox}}{T_{ox}} \]

\[ Q'_{sd}(max) = - q N_a x_{depletion} \]

\[ \text{Initial goal of inverting semiconductor surface} \]

\[ \text{was required bending of bands in semiconductor} \]

\[ \text{Making up for mismatch in work functions} \]

\[ V_{oxide} = - \left( Q_{total \ near \ semi \ surface} / C'_{ox} \right) \]

Final signs of each term will be VERY important. What are they?

\[ V_T = \]

\[ - \left( Q'_{depl} / C'_{ox} \right) - \left( Q'_{ss} / C'_{ox} \right) + \phi_{ms} + 2 \phi_{fp} \quad \text{(P-Semi / N-channel)} \]

\[ - \left( Q'_{depl} / C'_{ox} \right) - \left( Q'_{ss} / C'_{ox} \right) + \phi_{ms} - 2 \phi_{fn} \quad \text{(N-Semi / P-channel)} \]
Signs if use aluminum gate metal:

<table>
<thead>
<tr>
<th>$V_T$</th>
<th>plus</th>
<th>minus</th>
<th>minus</th>
<th>plus (P-Semi / N-channel)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>minus</td>
<td>minus</td>
<td>~ 0</td>
<td>minus (N-Semi / P-channel)</td>
</tr>
</tbody>
</table>

Proof of signs (starting from last)

a) $+2 \cdot \phi_{FP} / -2 \cdot \phi_{FN}$

$\phi_{FP} = (kT/q) \ln \left( \frac{N_a}{n_i} \right) > 0$ Thus $+2 \cdot \phi_{FP} = +$

$\phi_{FN} = (kT/q) \ln \left( \frac{N_d}{n_i} \right) > 0$ Thus $-2 \cdot \phi_{FN} = -$

b) $\phi_{ms}

$\phi_{ms} = \phi_m - \phi_{semi} = \phi_m - \phi_s$

$= \phi_m - \phi_{semi} - \left( \frac{E_g}{2q} + \phi_{FP} \right)$ P-type

$= \phi_m - \phi_{semi} - \left( \frac{E_g}{2q} + \phi_{FN} \right)$ N-type

For silicon: $\phi_{semi} = 4.01 \text{ eV}$ For aluminum: $\phi_m = 4.28 \text{ eV}$

Measured data (Streetman text / my website):

Put it all together for Aluminum gate and $Q_{SS}$ (Streetman text):

Term $E_g / 2 + q \phi_{FP}$ (for P-substrate) = top half of bandgap + offset of $E_F$ below mid bandgap:

- $E_g (\text{Al gate} / \text{P substrate})$
  - $\sim 4.28 \text{ V} - 4.01 \text{ V} - (-1.1 \text{ V}) = \text{negative}$

Term $E_g / 2 - q \phi_{FN}$ (for N-substrate) = top half of bandgap - offset of $E_F$ above mid bandgap:

- $E_g (\text{Al gate} / \text{N+ substrate})$
  - $\sim 4.28 \text{ V} - 4.01 \text{ V} - (0 \text{ V}) = \text{slightly positive}$
  - $\sim 0.1 \text{ eV} (\text{light doping})$

- $E_g (\text{Al gate} / \text{N- substrate})$
  - $\sim 4.28 \text{ V} - 4.01 \text{ V} - (0.1 \text{ V}) = 0 \text{ to negative}$

This is $V_T$ for REAL Al / SiO$_2$ / Si MOSFET:

- Voltage applied to metal (gate) layer to pull surface of underlying semiconductor through depletion
  and to the THRESHOLD of forming an INVERTED surface carrier channel
  that will electrically connect the source and drain wells ENHANCING the conductivity