BJTs
This is why a bipolar transistor is called bipolar.
If you could increase the minority carrier lifetime, this would be the effect on the common emitter gain, if everything else stayed the same.
If you reduce the collector doping and keep everything else the same, this would be the effect on the common emitter gain.
If you connected the base and collector leads together the resulting two-terminal device would act like this.
**True or False:** If you accidentally reversed the collector and emitter leads when building an amplifier circuit, it would still work.
Diodes

Return
True or False: in a forward-biased $n^+\text{-}p$ diode most of the current is carried by holes.
In an ideal forward-biased M-S diode, the resistance does this with increasing applied voltage. (increases, decreases, or stays the same)
In a reverse-biased ideal M-S diode, the capacitance does this with increasing applied voltage (increases, decreases, or stays the same).
In a p-n junction at equilibrium, this is where the electric field is the largest.
This is where most of the depletion layer is in a p+-n junction.
True or False: In an ideal p-n junction diode, the reverse bias current does not depend on the applied voltage for voltages greater than a few kT/q.
True or False: p-n junction diodes designed to have a fast switching time also have large reverse bias currents.
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AC
The C-V plot ($1/C^2$ vs $V$) for a p-n junction in forward bias diode can be used to determine this.
The C-V plot \((1/C^2 \text{ vs } V)\) for an M-S diode (rectifying) can be used to determine this.
These are the two mechanisms used to remove the stored charge in a p-n junction diode when switched from forward to reverse bias.
This is the main reason that M-S diodes usually have faster switching times than p-n junction diodes.
If a reverse biased M-S (rectifying) diode has 10pF capacitance at -2 V, this is the value of the capacitance for 2V forward bias on the same device.
True or False: The Schottky barrier height is a function of the semiconductor doping.
If $\varphi_m > \varphi_s$ and contact is made to a nondegeneratively doped n-type substrate, this is the type of contact that will be formed.
If $\varphi_m > \varphi_s$ and contact is made to a nondegeneratively doped p-type substrate, this is the type of contact that will be formed.
True or False: The dominant current carriers in an M-S diode are minority carriers.
MOSFETS
In a MOS diode, the capacitance is at a minimum at or near this voltage.
True or False: If the gate voltage is above the threshold voltage for an ideal NMOS-FET, there is no steady-state gate current.
**True or False:** If the gate voltage is below the threshold voltage for an ideal NMOS-FET, the Source-to-Drain current is independent of the drain-source voltage.
The magnitude of the threshold voltage for a MOSFET would do this if the substrate doping was decreased.
If you accidentally reversed the source and drain leads on a MOSFET, this would be the effect on the output characteristics such as transconductance, $g_m$. 

Return
If the threshold voltage of a MOSFET steadily declines over a long period of time, this is the likely cause.
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It takes this polarity of gate voltage to invert a MOS capacitor made with an n-type silicon substrate.
True or False: The minimum capacitance of an ideal MOS capacitor occurs for zero applied volts.
When the bias on an MOS-C is changed from just above to just below the threshold for inversion, it takes about this long for the inversion layer charge to go away.
Of the following, this is the only quantity that cannot be determined from a C-V curve for an MOS-C: minority carrier lifetime, oxide trapped charge, threshold voltage, oxide thickness, gate metal work function, or flat band capacitance.
For an MOS-C, a C-V curve that is distorted in shape (stretched out) is an indication of the presence of these.
The mobility of carriers does this as the gate voltage is increased above the threshold voltage.
If the measured threshold voltage of a MOSFET is different from the value calculated from the design/fabrication parameters, *this* is likely the cause.
This is the reason for using high-K oxides
This is the reason for using strained Si channels
This is the reason for using raised S-D
This is the reason for using LDD
This is the reason for using Halo Doping
This is the reason for using shallow junctions
This is the mechanism of current conduction for ohmic contacts formed on heavily doped semiconductor substrates such as the source and drain of a NMOS transistor.
RG
This is a mechanism for generation of electron-hole pairs when large voltages are applied to a semiconductor.
This diagram represents a semiconductor under this condition.
This diagram represents a semiconductor under this condition.
This is what is meant by the flat band condition when describing surface recombination velocity.
Indirect bandgap semiconductors like silicon are not very efficient at emitting photons but can be very efficient at absorbing them. This is why.